Summary of work done at CARES( 5/28/2015 ~ 11/13/15)

Computer Architecture review (1 semesters worth of class @ SNU, 6 weeks)

* Course was done in BlueSpec Verilog and Y86 assembly code
* Some of the courseload included constructing a fully functioning 5 stage pipeline with branch prediction and data cache
  + Done in BlueSpec Verilog

Computer Architecture Modification

* Translation of existing projects and assignments from previous class to Y86-64 (a new language)
* Reconstruction of all course source files and supplementary files
  + Mostly done in assembly code and hexadecimal code
* Implementation of an instruction cache using virtual memory
* Extensive testing to prevent corner cases in the projects
* Fixed project introduction files using LaTeX
* Creation of new tests in hexadecimal code to counter new corner cases from 64 bit assembly code
* Optimization and abstraction of code

Connectal and FPGAs

* Utilized the Connectal framework developed by MIT CSAIL
  + A framework to make hardware/software programming and integration much easier by creating portals that could transfer requests and information from the user space to the hardware/flash
* Created a simple program to demonstrate its effects

Data organization

* Created multiple python script to organize a large amount of kernel logs
* Optimized and easily customizable
* Not too complicated

App development

* Created an android application that runs commands on adb for kernel logging purposes (completely for testing purposes for OS logs)
  + Generates errors if applicable etc.
* Used Android Studio

Paper revision

* Proofread papers that concerned setting erase modes for NAND based memory to improve endurance(DeVTS)
* No participation in research, only proofreading the English